**Digital Logics Lab sheet Manual**

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| **Lab No** | **Topics** |  |  |
| 1 | Verification of AND Gate |  |  |
| 2 | Verification of OR Gate |  |  |
| 3 | Verification of NOT Gate |  |  |
| 4 | Verification of NAND Gate |  |  |
| 5 | Verification of NOR Gate |  |  |
| 6 | Verification of XOR Gate |  |  |
| 7 | Verification of XNOR Gate |  |  |
| 8 | Verification of NAND as NOT Gate |  |  |
| 9 | Verification of NAND as AND Gate |  |  |
| 10 | Verification of NAND as OR Gate |  |  |
| 11 | Verification of NOR as NOT Gate |  |  |
| 12 | Verification of NOR as AND Gate |  |  |
| 13 | Verification of NOR as OR Gate |  |  |
| 14 | Verification of Half Adder |  |  |
| 15 | Verification of Full Adder |  |  |
| 16 | Verification of Half Subtractor |  |  |
| 17 | Verification of Full Subtractor |  |  |
| 18 | Verification of 3-8 Decoder |  |  |
| 19 | Verification of 4x1 MUX |  |  |
| 20 | Implementation of 7 Segment Display |  |  |